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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,453	12/24/2001	Paul Gerard D'Arcy	13-1	1909

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,453	D'ARCY ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 15 recites, "the add-compare-select algorithm is implemented in accordance with an integrated circuit device", which is incomprehensible since an add-compare-select algorithm is an algorithm and it is not clear how an algorithm can be based on an integrated circuit.

Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between "the add-compare-select algorithm" and "an integrated circuit device".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 7, 10, 12, 15, 16 and 19 rejected under 35 U.S.C. 102(e) as being anticipated by Yamanaka; Ryutaro et al. (US 6330684 B1, hereafter referred to as Yamanaka).

35 U.S.C. 102(e) rejection of claims 1, 7, 12, 15, 16 and 19.

Yamanaka teaches a method of performing add-compare-select operations in accordance with a Viterbi decoder (see Figure 6 of Yamanaka; col. 1, lines 11-18 in Yamanaka teach that a digital signal processor is used to implement the Viterbi decoder), the method comprising the steps of: respectively adding input values of two or more sets of input values to generate sums for the two or more sets (Adding Sections 6 and 10 in Figure 6 of Yamanaka perform the step of adding input values of two or more sets of input values to generate sums for the two or more sets; Note: a set of a single element is still a set); substantially concurrent with the respective addition of the input values of the two or more sets of input values, comparing the two or more sets of input values (Comparing Section 5 and 9 Figure 6 of Yamanaka substantially concurrent with the respective addition of the input values of the two or more sets of input values, comparing the two or more sets of input values); and selecting one of the generated sums of the two or more input sets based on the comparison of the two or more sets of input values (Selecting Sections 8 and 12 of Yamanaka teach the step of selecting one of the generated sums of the two or more input sets based on the comparison of the two

or more sets of input values). Comparison Result Storing Sections 7 and 11 in Figure 6 of Yamanaka is a memory, coupled to the at least one processor for processing Branch Metrics, for storing at least a portion of results associated with one or more of the add, compare, select operations.

35 U.S.C. 102(e) rejection of claims 5 and 10.

The device of Figures 6 and 18 of Yamanaka is a device for performing the add-compare-select algorithm for a Viterbi decoder which is an algorithm wherein one input value of each set of input values is a previously computed path metric and the other input value of each set of input values is an appropriate branch metric such that the generated sum of the input values represents a new path metric which may potentially be selected based on the substantially concurrent comparison operation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka; Ryutaro et al. (US 6330684 B1, hereafter referred to as Yamanaka).

35 U.S.C. 103(a) rejection of claims 2, 8, 13, 17 and 20.

Yamanaka substantially teaches the claimed invention described in claims 1, 7, 12, 16 and 19 (as rejected above).

However Yamanaka does not explicitly teach the specific use of determining which set of the two or more sets would result in the largest sum.

The Examiner asserts that branch metrics a measure of accuracy of a particular path and during comparison the best branch metric is kept and stored. It is an obvious engineering design choice to select an embodiment with either increasing or decreasing values of branch metrics used to denote the better or best branch metric to keep. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yamanaka by including use of determining which set of the two or more sets would result in the largest sum. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of determining which set of the two or more sets would result in the largest sum would have provided the opportunity to impalement an embodiment of the teachings in

the Yamanaka patent whereby either increasing or decreasing values of branch metrics used to denote the better or best branch metric to keep.

35 U.S.C. 103(a) rejection of claims 3, 9, 14, 18 and 21.

Col. 13, lines 25-31 in Yamanaka teach that a carry operation is performed at comparator 26 of Figure 18 in Yamanaka and the results of the comparator are used to determine, which set of the two or more sets would result in the largest sum.

35 U.S.C. 103(a) rejection of claim 4.

Claim 11 in Yamanaka teaches at least one of said two comparators in Figures 6 and 18 of Yamanaka is a compressor and an arithmetic operation device.

35 U.S.C. 103(a) rejection of claims 6 and 11.

Yamanaka substantially teaches the claimed invention described in claims 1, 7, 12, 16 and 19 (as rejected above). Note: Figure 6 in Yamanaka teaches that the input values of the two or more sets are available to the comparison operation before completion of the addition operation.

However Yamanaka does not explicitly teach the specific use of completing the comparison operation before completion of the addition operation.

The Examiner asserts that it would be an obvious engineering design choice to use faster logic for the comparing section of Figure 6 in Yamanaka since the output from the

comparing section is required at the selecting circuit prior to the arrival of the output from the adding sections in Figure 6.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yamanaka by including use of completing the comparison operation before completion of the addition operation. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of completing the comparison operation before completion of the addition operation would have provided the opportunity to ensure the arrival of the output from the comparing section before or upon arrival of the output from the adding sections in Figure 6.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cideciyan; Roy Daron et al. (US 6373906 B1) teaches Viterbi detection of generalized partial response signals using transformed metrics, such as the partial matched filter branch metrics and the matched filter branch metrics and including two-way add/compare/select for improved channel speed. Lee; Inkyu et al. (US 6148431 A) teaches Add-Compare-Select (ACS) circuitry implementing a Viterbi algorithm. Fredrickson; Lyle J. et al. (US 5327440 A) teaches Viterbi trellis coding methods and apparatus for partial-response maximum-likelihood (PRML) data channels

in a direct access storage device (DASD). Tong; Mui-Chwee et al. (US 6298464 B1) teaches maximum likelihood sequence detection in a Viterbi decoder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133